1. (amended) A photodetector array comprising a plurality of addressable pixels, each pixel comprising:

at least two photodiodes;

a switching circuit which allows switching of at least one of said photodiodes between a first circuit and a second circuit;

wherein said first circuit directly combines the outputs of said at least two photodiodes in parallel, and said second circuit directly combines the output of said at least one of said photodiodes in parallel with the output of a photodiode of a neighboring pixel in the array, whereby said array is switchable between a high resolution and a low resolution pixel configuration, said pixel having an intrinsic capacitance which stores said combined photodiode outputs prior to their being read out, and

an addressing circuit which enables the combined photodiode outputs stored on said pixel's intrinsic capacitance to be read out in response to an address input.

8. (amended) A photodetector array with selectable resolution, comprising:

a plurality of photodetectors;

a switching circuit which configures neighboring ones of said photodetectors into pixels by directly summing at each pixel the outputs of multiple photodetectors into an aggregated pixel output, said aggregated pixel output stored on said pixel's intrinsic capacitance prior to being read out;

wherein said switching circuit is electronically switchable to aggregate said photodetector signals according to at least two different selectable pixellization schemes with differing resolutions, and

a plurality of addressable interface circuits, each of which enables the aggregated pixel output stored on a respective one of said pixel's to be read out in response to an address

input.

12. (amended) A photodetector array, comprising a plurality of pixels;

wherein each pixel comprises an association of at least two subpixels;

and wherein the outputs of said subpixels are switchably combined into at least two different grouping arrangements, to give at least two different selectable pixel configurations,

each of said pixels having an intrinsic capacitance which stores said combined subpixel outputs prior to their being read out, and

an addressing circuit which enables the combined subpixel outputs stored on said pixel's intrinsic capacitance to be read out in response to an address input.

Please add claim 15 as follows:

15. The photodetector array of claim 12, wherein said array of pixels comprises a plurality of pixels arranged into at least three horizontal rows and vertical columns,

wherein said at least two different grouping arrangements comprises two different grouping arrangements, one of which combines the outputs of two adjacent subpixels in a given vertical column, and the other of which combines the outputs of three adjacent subpixels in said given vertical column.

REMARKS

This amendment is in response to the Office Action dated 1/30/02. Entry of this Amendment and reconsideration of this application are respectfully requested.